

## CLAIMS

- 1 1. A signal modulation circuit for modulating a differential pulse width modulation  
2 signal, comprising:  
3 a first channel signal processing element having an input coupled for receiving a first  
4 channel of the differential signal, an output, and a control signal output;  
5 a second channel signal processing element having an input coupled for receiving a  
6 second channel of the differential signal, an output, and a control signal  
7 output;  
8 a first logic gate having a first input coupled to the output of said first channel signal  
9 processing element, a second input coupled to the output of said second  
10 channel signal processing element, and an output;  
11 a second logic gate having a first input coupled to the control signal output of said  
12 first channel signal processing element, a second input coupled to the  
13 control signal output of said second channel signal processing element, a  
14 third input coupled to the output of said first logic gate, and an output;  
15 a first switch having a first electrode coupled to the output of said first channel signal  
16 processing element, a second electrode coupled for transmitting a first  
17 channel of an output signal, and a control electrode coupled to the output of  
18 said second logic gate; and  
19 a second switch having a first electrode coupled to the output of said second channel  
20 signal processing element, a second electrode coupled for transmitting a  
21 second channel of the output signal, and a control electrode coupled to the  
22 output of said second logic gate.
- 1 2. The signal modulation circuit of claim 1, wherein:  
2 said first switch includes a first logic AND gate having a first input coupled to the  
3 output of said first channel signal processing element, a second input  
4 coupled to the output of said second logic gate, and an output coupled for  
5 transmitting the first channel of the output signal; and  
6 said second switch includes a second logic AND gate having a first input coupled to  
7 the output of said second channel signal processing element, a second input  
8 coupled to the output of said second logic gate, and an output coupled for  
9 transmitting the second channel of the output signal.

- 1 3. The signal modulation circuit of claim 1, said first channel signal processing element  
2 comprising:  
3 a first delay gate having an input and an output coupled to the input and the output,  
4 respectively, of said first channel signal processing element;  
5 a second delay gate having an input coupled to the input of said first channel signal  
6 processing element and an output;  
7 a first storage element having a first input and a second input coupled to the input  
8 and the output, respectively, of said first delay gate, and an output;  
9 a second storage element having a first input and a second input coupled to the  
10 outputs of said first delay gate and said second delay gate, respectively, and  
11 an output; and  
12 a logic gate having a first input and a second input coupled to the outputs of said first  
13 and second storage elements, respectively, and an output coupled to the  
14 control signal output of said first channel signal processing element.
- 1 4. The signal modulation circuit of claim 1, wherein said first logic gate includes a logic  
2 AND gate and said second logic gate includes a logic NAND gate.
- 1 5. The signal modulation circuit of claim 1, said second channel signal processing  
2 element comprising:  
3 a first delay gate having a first delay time and having an input coupled to the input of  
4 said second channel signal processing element and an output coupled to the  
5 output of said second channel signal processing element;  
6 a second delay gate having a second delay time different from the first delay time  
7 and having an input coupled to the input of said second channel signal  
8 processing element and an output;  
9 a first bistable gate having a data input coupled to the input of said second channel  
10 signal processing element, a reset input coupled to the output of said first  
11 delay gate, and an inverted output;  
12 a second bistable gate having a first input coupled to the output of said first delay  
13 gate, a second input coupled to the output of said second delay gate, and an  
14 inverted output; and  
15 a logic AND gate having a first input coupled to the inverted output of said first  
16 bistable gate, a second input coupled to the inverted output of said second  
17 bistable gate, and an output coupled to the control signal output of said  
18 second channel signal processing element.
- 1 6. The signal modulation circuit of claim 5, said second channel signal processing  
2 element further comprising:  
3 a first inverter coupled between the input of said second channel signal processing  
4 element and the data input of said first bistable gate; and

5 a second inverter coupled between the output of said first delay gate and the reset  
6 input of said first bistable gate.

1 7. The signal modulation circuit of claim 1, further comprising a zero differential mode  
2 signal detection element having first and second inputs coupled to the outputs of said  
3 first and second channel signal processing elements, respectively, and an output  
4 coupled to said second logic gate.

1 8. A nonlinear amplifier, comprising:  
2 a transform logic circuit coupled for receiving a differential signal and including:  
3 a logic AND gate coupled for receiving the differential signal and  
4 configured to generate an output signal at an output thereof and at a  
5 first logic level in response to first and second components of the  
6 differential signal being at the first logic level;  
7 a first processing element and a second processing element, each coupled  
8 for receiving a corresponding component of the differential signal  
9 and configured to generate a corresponding control signal at the  
10 first logic level and switching to a second logic level for a  
11 predetermined time interval following a rising edge and preceding  
12 a falling edge in the corresponding component of the differential  
13 signal; and  
14 a switching element having first and second inputs coupled for receiving a  
15 corresponding component of the differential signal and first and  
16 second outputs, said switching element being conductive between  
17 the first input and output and between the second input and output  
18 in response to at least one of the first control signal, the second  
19 control signal, and the output signal of said logic AND gate being  
20 at the second logic level; and  
21 a switching bridge having first and second control terminals coupled to the first and  
22 second outputs, respectively, of said switching element in said transform  
23 logic circuit.

1 9. The nonlinear amplifier of claim 8, wherein each of said first processing element and  
2 said second processing element in said transform logic circuit includes:  
3 a first delay gate having a first delay time and having an input coupled for receiving  
4 a corresponding component of the differential signal and an output coupled  
5 to a corresponding input of said switching element;  
6 a second delay gate having a second delay time and having an input coupled to the  
7 input of said first delay gate and an output;  
8 a first bistable gate having a first input coupled to the input of said first delay gate, a  
9 second input coupled to the output of said first delay gate, and an output;

10 a second bistable gate having a first input coupled to the output of said first delay  
11 gate, a second input coupled to the output of said second delay gate, and an  
12 output; and  
13 an AND gate having a first input coupled to the output of said first bistable gate, a  
14 second input coupled to the output of said second bistable gate, and an  
15 output.

1 10. The nonlinear amplifier of claim 9, wherein each of said first processing element and  
2 said second processing element in said transform logic circuit further includes a first  
3 inverter coupled between the input of said first delay gate and the first input of said  
4 first bistable gate and a second inverter coupled between the output of said first delay  
5 gate and the second input of said first bistable gate.

1 11. The nonlinear amplifier of claim 9, wherein said switching element in said transform  
2 logic circuit includes:  
3 a logic NAND gate having a first input coupled to the output of said AND gate in  
4 said first processing element, a second input coupled to the output of said  
5 AND gate in said second processing element, a third input coupled to the  
6 output of said logic AND gate, and an output;  
7 a first AND gate having a first input coupled to the output of said first delay gate in  
8 said first processing element, a second input coupled to the output of said  
9 logic NAND gate, and an output coupled to the first control terminal of said  
10 switching bridge; and  
11 a second AND gate having a first input coupled to the output of said first delay gate  
12 in said second processing element, a second input coupled to the output of  
13 said logic NAND gate, and an output coupled to the second control terminal  
14 of said switching bridge.

1 12. The nonlinear amplifier of claim 11, said transform logic circuit further including a  
2 zero signal detection element having first and second inputs coupled to the outputs of  
3 said first delay gates in said first and second processing elements, respectively, and  
4 an output coupled to said logic NAND gate.

1 13. The nonlinear amplifier of claim 9, wherein:  
2 the first delay time of said first delay gate in each of said first processing element and  
3 said second processing element in said transform logic circuit is  
4 substantially equal to the predetermined time interval; and  
5 the second delay time of said second delay gate each of said first processing element  
6 and said second processing element in said transform logic circuit is  
7 substantially equal to twice of the predetermined time interval.

1 14. The nonlinear amplifier of claim 8, said switching bridge including:

2 a first switch having a control electrode coupled to the first output of said switching  
 3 element in said transform logic circuit, a first current conducting electrode  
 4 coupled to a first voltage level, and a second current conducting electrode  
 5 coupled to a first output terminal of the nonlinear amplifier;  
 6 a second switch having a control electrode coupled to the control electrode of said  
 7 first switch, a first current conducting electrode coupled to a second voltage  
 8 level, and a second current conducting electrode coupled to the second  
 9 current conducting electrode of said first switch;  
 10 a third switch having a control electrode coupled to the second output of said  
 11 switching element in said transform logic circuit, a first current conducting  
 12 electrode coupled to the first voltage level, and a second current conducting  
 13 electrode coupled to a second output terminal of the nonlinear amplifier; and  
 14 a fourth switch having a control electrode coupled to the control electrode of said  
 15 third switch, a first current conducting electrode coupled to the second  
 16 voltage level, and a second current conducting electrode coupled to the  
 17 second current conducting electrode of said third switch.

1 15. The nonlinear amplifier of claim 14, wherein:  
 2 said first switch includes a first pull-up field effect transistor;  
 3 said second switch includes a first pull-down field effect transistor;  
 4 said third switch includes a second pull-up field effect transistor; and  
 5 said fourth switch includes a second pull-down field effect transistor.

1 16. A signal modulation process, comprising the steps of:  
 2 providing a differential signal having a first channel and a second channel;  
 3 generating a first control signal and a second control signal at a first logic level;  
 4 switching the first control signal to a second logic level for a predetermined time  
 5 interval following a rising edge and preceding a falling edge in the first  
 6 channel of the differential signal;  
 7 switching the second control signal to the second logic level for the predetermined  
 8 time interval following a rising edge and preceding a falling edge in the  
 9 second channel of the differential signal; and  
 10 generating a modified signal by blocking a transmission of the differential signal in  
 11 response to the first and second channels of the differential signal being at  
 12 logic high and the first and second control signals at the first logic level.

1 17. The signal modulation process of claim 16, wherein the step of switching the first  
 2 control signal to a second logic level for a predetermined time interval following a  
 3 rising edge and preceding a falling edge in the first channel of the differential signal  
 4 further includes the steps of:  
 5 generating a first delayed signal by delaying the first channel of the differential  
 6 signal by the predetermined time interval;

7 generating a second delayed signal by delaying the first channel of the differential  
8 signal by two times of the predetermined time interval;  
9 generating a first logic signal and a second logic signal at the first logic level;  
10 in response to a rising edge in the first delayed signal, switching the first logic signal  
11 to the second logic level;  
12 in response to a rising edge in the second delayed signal, switching the first logic  
13 signal back to the first logic level;  
14 in response to a falling edge in the first channel of the differential PWM, switching  
15 the second logic signal to the second logic level;  
16 in response to a falling edge in the first delayed signal, switching the second logic  
17 signal back to the first logic level; and  
18 generating the first control signal at the first logic level in response to the first logic  
19 signal and the second logic signal at the first logic level and at the second  
20 logic level in response to at least one of the first logic signal and the second  
21 logic signal at the second logic level.

1 18. The signal modulation process of claim 17, wherein the step of generating a modified  
2 signal further includes the steps of:  
3 generating a third control signal at the first logic level in response to the first delayed  
4 signal corresponding to the first channel of the differential signal and a first  
5 delayed signal corresponding to the second channel of the differential signal  
6 at the first logic level and at the second logic level in response to at least one  
7 of the first delayed signals corresponding to the first and second channels of  
8 the differential signal at the second logic level;  
9 transmitting the first delayed signals corresponding to the first and second channels  
10 of the differential signal in response to at least one of the first, second, and  
11 third control signals at the second logic level; and  
12 blocking the first delayed signals corresponding to the first and second channels of  
13 the differential signal in response to the first, second, and third control  
14 signals at the first logic level.

1 19. The signal modulation process of claim 16, wherein the step of generating a modified  
2 signal further includes the step of blocking the differential signal in response to a  
3 difference between the first and second channels of the differential signal being less  
4 than a predetermined value.

1 20. The signal modulation process of claim 16, further comprising the step of  
2 transmitting the modified signal to a switching bridge in a nonlinear amplifier.